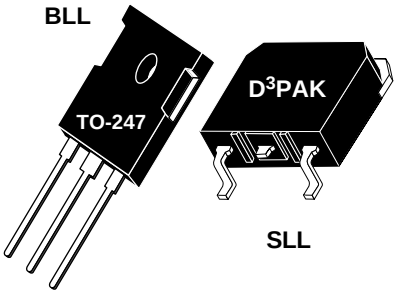
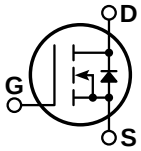
APT5018BLL
APT5018SLL
500V 27A 0.180Ω

POWER MOS 7® MOSFET



Power MOS 7® is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7® by significantly lowering $R_{DS(ON)}$ and Q_g. Power MOS 7® combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.

- **Lower Input Capacitance**
- **Lower Miller Capacitance**
- **Lower Gate Charge, Qg**
- **Increased Power Dissipation**
- **Easier To Drive**
- **TO-247 or Surface Mount D³PAK Package**



MAXIMUM RATINGS All Ratings: T_C = 25°C unless otherwise specified.

Symbol	Parameter	APT5018	UNIT
V_{DSS}	Drain-Source Voltage	500	Volts
I_D	Continuous Drain Current @ T_C = 25°C	27	Amps
I_{DM}	Pulsed Drain Current ①	108	
V_{GS}	Gate-Source Voltage Continuous	±30	Volts
V_{GSM}	Gate-Source Voltage Transient	±40	
P_D	Total Power Dissipation @ T_C = 25°C	300	Watts
	Linear Derating Factor	2.4	W/°C
T_J,T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ① (Repetitive and Non-Repetitive)	27	Amps
E_{AR}	Repetitive Avalanche Energy ①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ④	1210	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage (V_{GS} = 0V, I_D = 250μA)	500			Volts
$I_{D(on)}$	On State Drain Current ② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, V_{GS} = 10V)	27			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ② (V_{GS} = 10V, 13.5A)			0.18	Ohms
I_{DSS}	Zero Gate Voltage Drain Current (V_{DS} = 500V, V_{GS} = 0V)			100	μA
	Zero Gate Voltage Drain Current (V_{DS} = 400V, V_{GS} = 0V, T_C = 125°C)			500	
I_{GSS}	Gate-Source Leakage Current (V_{GS} = ±30V, V_{DS} = 0V)			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1mA)	3		5	Volts

CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

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DYNAMIC CHARACTERISTICS

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1 MHz		2596		pF
C_{oss}	Output Capacitance			546		
C_{rss}	Reverse Transfer Capacitance			38		
Q_g	Total Gate Charge ③	V_{GS} = 10V V_{DD} = 250V I_D = 27A @ 25°C		58		nC
Q_{gs}	Gate-Source Charge			15		
Q_{gd}	Gate-Drain ("Miller") Charge			31		
$t_{d(on)}$	Turn-on Delay Time	**RESISTIVE SWITCHING** V_{GS} = 15V V_{DD} = 250V I_D = 27A @ 25°C R_G = 1.6Ω		9		ns
t_r	Rise Time			4		
$t_{d(off)}$	Turn-off Delay Time			18		
t_f	Fall Time			2		
E_{on}	Turn-on Switching Energy ⑥	**INDUCTIVE SWITCHING @ 25°C** V_{DD} = 333V, V_{GS} = 15V I_D = 27A, R_G = 5Ω		216		µJ
E_{off}	Turn-off Switching Energy			134		
E_{on}	Turn-on Switching Energy ⑥	**INDUCTIVE SWITCHING @ 125°C** V_{DD} = 333V V_{GS} = 15V I_D = 27A, R_G = 5Ω		337		
E_{off}	Turn-off Switching Energy			162		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			27	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			100	
V_{SD}	Diode Forward Voltage ② (V_{GS} = 0V, I_S = -I_D27A)			1.3	Volts
t_{rr}	Reverse Recovery Time (I_S = -I_D27A, dI_S/dt = 100A/µs)		544		ns
Q_{rr}	Reverse Recovery Charge (I_S = -I_D27A, dI_S/dt = 100A/µs)		8		µC
$^{dv}/_{dt}$	Peak Diode Recovery $^{dv}/_{dt}$ ⑤			8	V/ns

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.42	°C/W
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature
② Pulse Test: Pulse width < 380 µs, Duty Cycle < 2%
③ See MIL-STD-750 Method 3471
④ Starting T_j = +25°C, L = 3.32mH, R_G = 25Ω, Peak I_L = 27A
⑤ $^{dv}/_{dt}$ numbers reflect the limitations of the test circuit rather than the device itself. $I_S \le -I_D27A$ $^{di}/_{dt} \le 700A/\mu s$ $V_R \le V_{DSS}$ $T_J \le 150°C$
⑥ Eon includes diode reverse recovery. See figures 18, 20.

APT Reserves the right to change, without notice, the specifications and information contained herein.

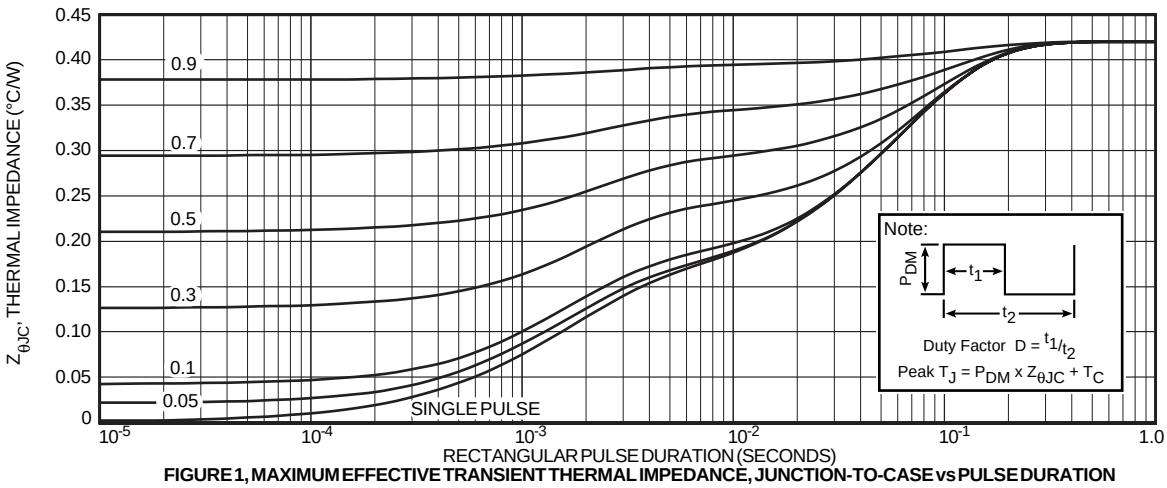


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

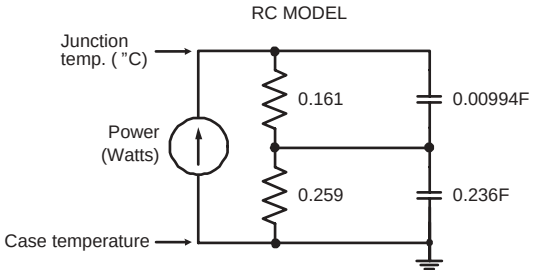


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

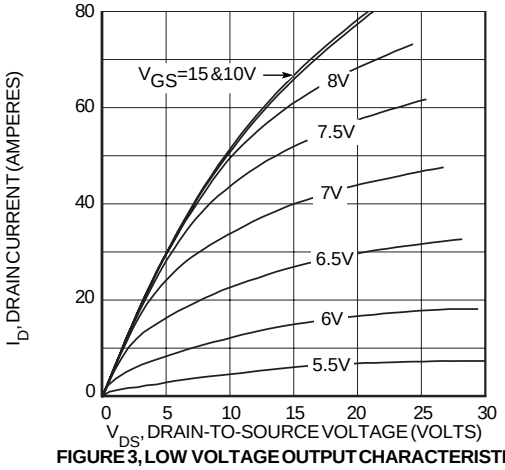


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

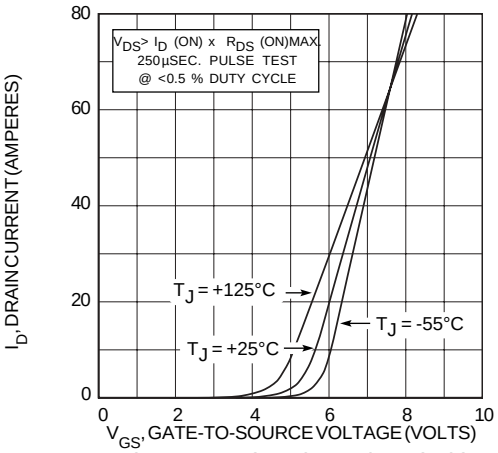


FIGURE 4, TRANSFER CHARACTERISTICS

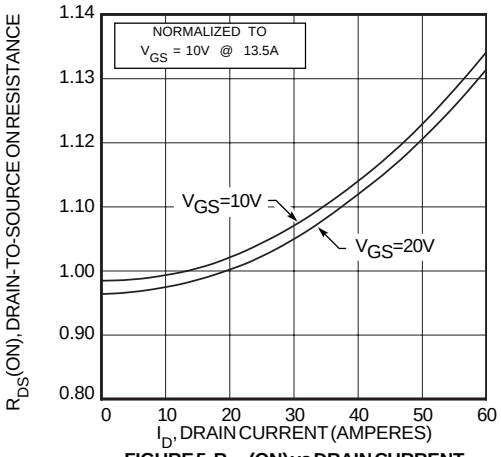


FIGURE 5, R_{DS}(ON) vs DRAIN CURRENT

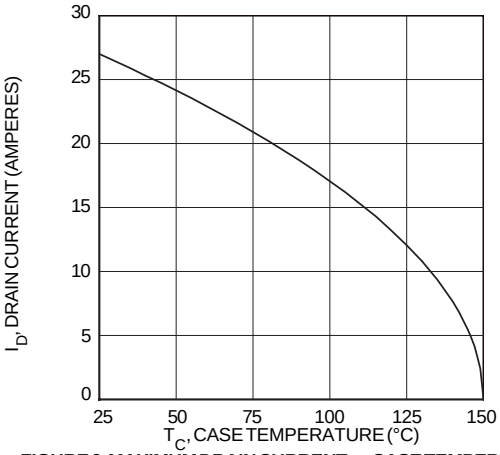


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

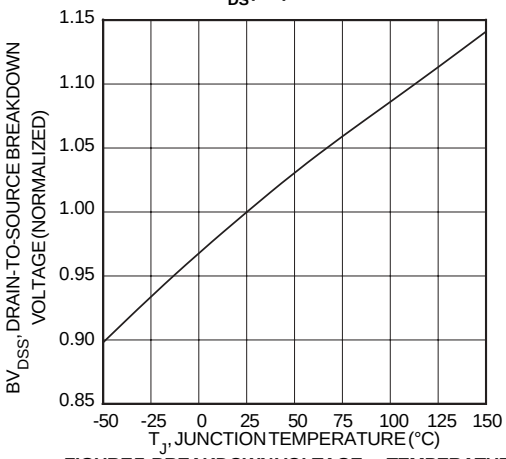


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

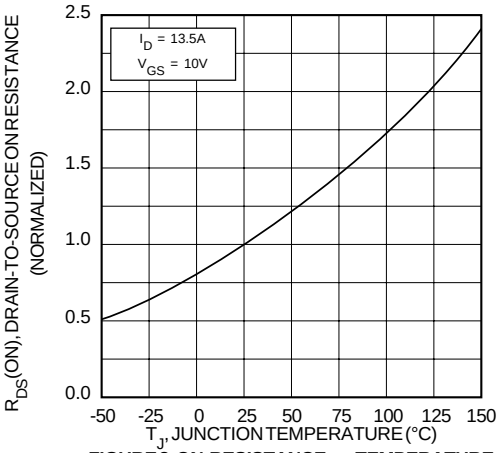


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

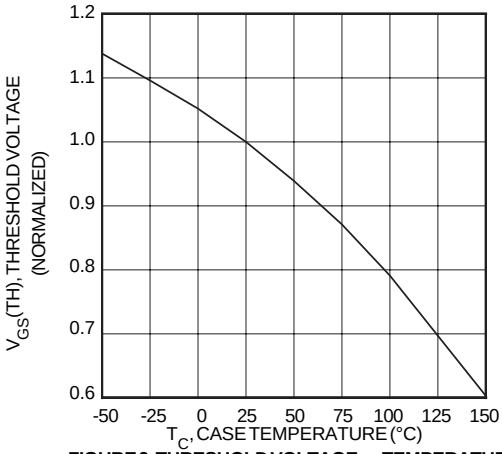


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

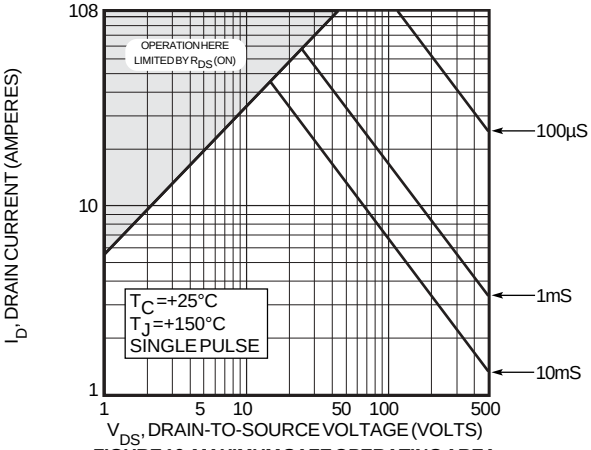


FIGURE 10, MAXIMUM SAFE OPERATING AREA

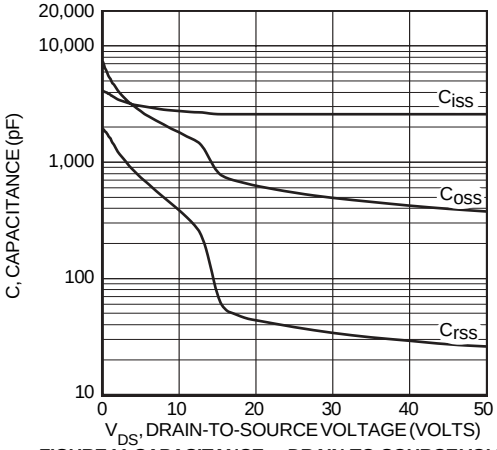


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

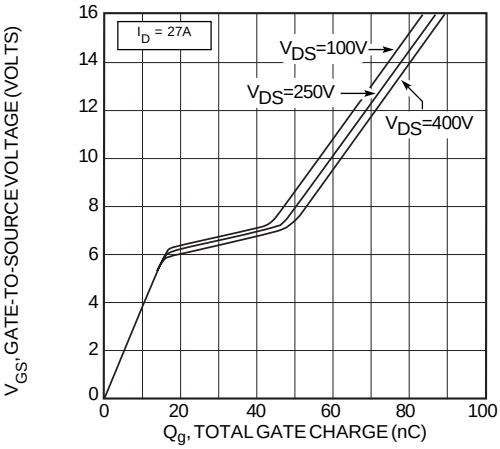


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

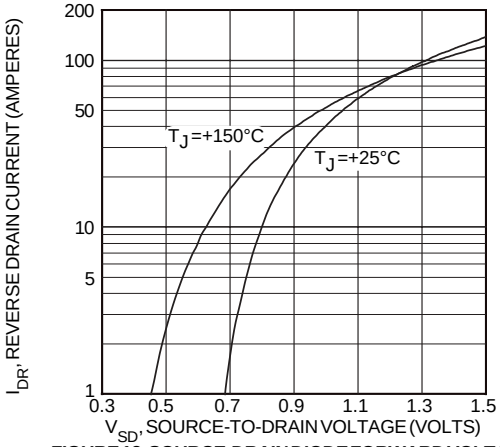


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

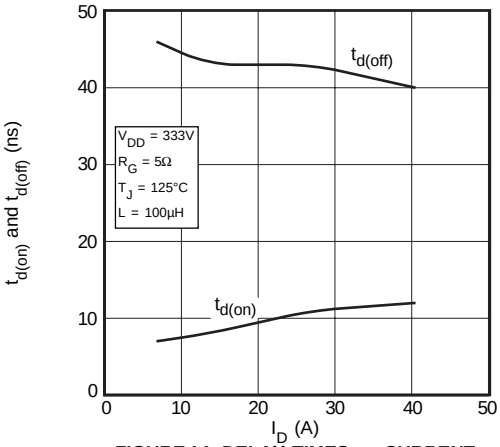


FIGURE 14, DELAY TIMES vs CURRENT

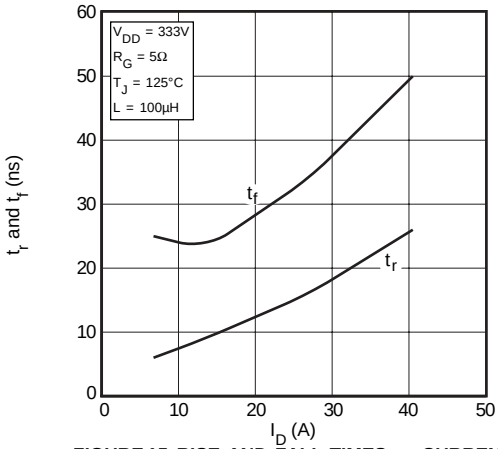


FIGURE 15, RISE AND FALL TIMES vs CURRENT

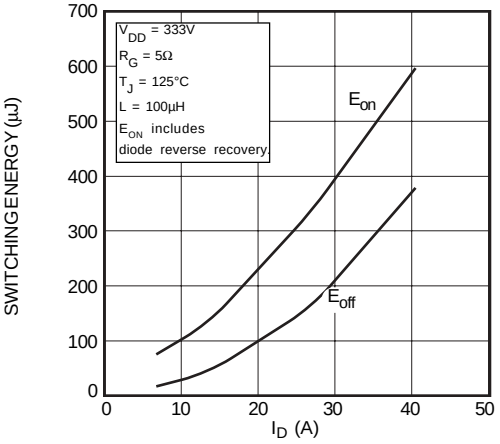


FIGURE 16, SWITCHING ENERGY vs CURRENT

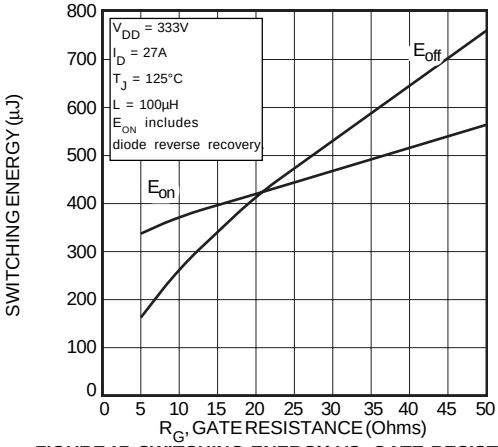


FIGURE 17, SWITCHING ENERGY VS. GATE RESISTANCE

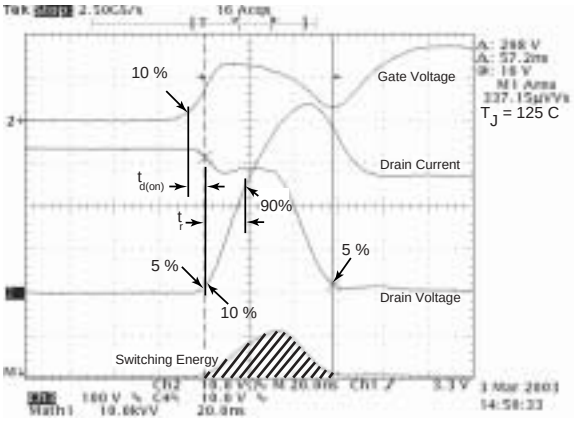


Figure 18, Turn-on Switching Waveforms and Definitions

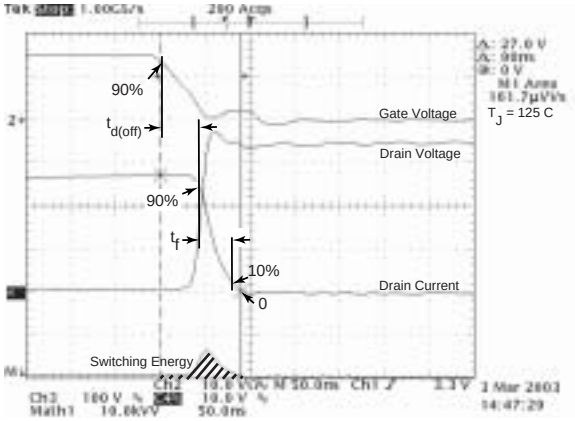


Figure 19, Turn-off Switching Waveforms and Definitions

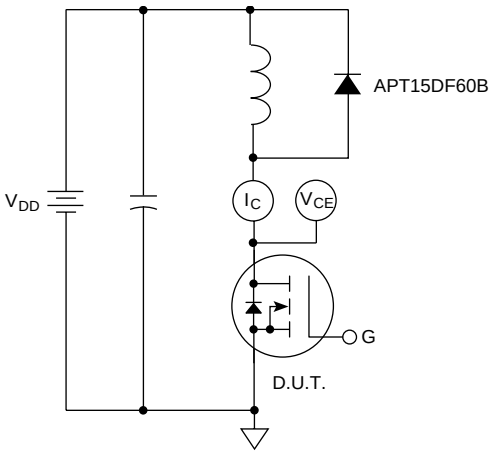
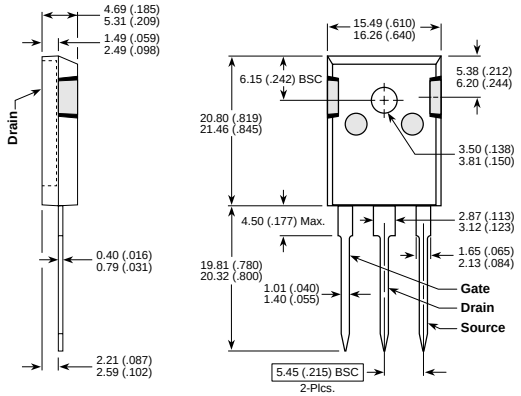


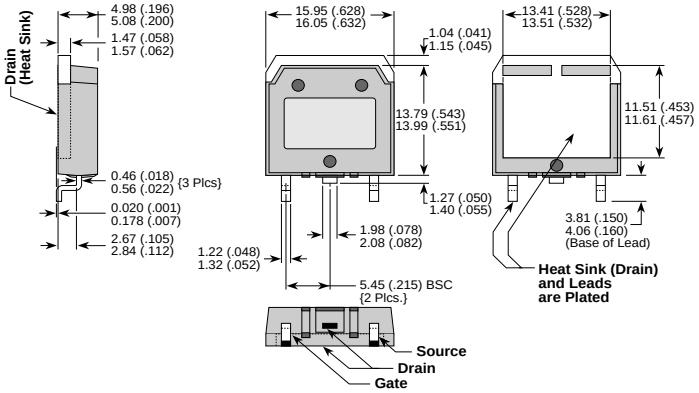
Figure 20, Inductive Switching Test Circuit

TO-247 Package Outline



Dimensions in Millimeters and (Inches)

D^{3}PAK Package Outline



Dimensions in Millimeters (Inches)

APT's products are covered by one or more of U.S.patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522
5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 and foreign patents. US and Foreign patents pending. All Rights Reserved.